

All-Digital Single Sideband (SSB) Bluetooth Low Energy (BLE) Backscatter with an Inductor-free, Digitally-Tuned Capacitance Modulator

James Rosenthal¹ and Matthew S. Reynolds
 Department of Electrical & Computer Engineering
 University of Washington
 Seattle, WA, USA
¹jamesdroenthal@gmail.com

Abstract—We present a novel all-digital approach for generating single-sideband (SSB) backscatter communication uplinks, using an inductor-free, digitally-tuned capacitance modulator. An example Bluetooth Low Energy (BLE) compatible single-sideband backscatter implementation is described. The FPGA-based approach presented here consumes 35.5 mW, of which 34.8 mW (98.2%) is due to digital logic in the FPGA, and only 600 μ W (1.8%) is consumed by the backscatter modulator. The measured sideband suppression ratio is 10.7 dB. Over-the-air tests demonstrate compatibility with a completely unmodified (neither hardware nor software modifications) iPad, iPhone, Samsung Android Smartphone, and an off-the-shelf BLE chipset from Nordic Semiconductor. This all-digital approach points the way toward future single-chip, inductor-free SSB BLE-compatible backscatter sensors and devices.

Keywords—backscatter communication, RFID, brain-computer interfaces, biomedical implants.

I. INTRODUCTION

Backscatter radios have the potential to dramatically reduce the size, weight, and power consumption of wireless uplinks for embedded systems, improving battery life and even eliminating the need for batteries entirely in devices like the implanted biomedical devices shown in Fig. 1 and [1], [2]. Backscatter radios achieve these simplicity and energy efficiency advantages by removing the energy hungry functions of RF carrier generation and RF amplification from the energy-constrained device. The continuous wave (CW) carrier needed by the backscatter device is instead provided by an energy-rich external source, and the backscatter radio uplinks data by selectively reflecting the external CW carrier via changing the impedance presented to its antenna.

Prior work describes several backscatter modulation approaches. Using an RF switch to switch among multiple impedances, it is possible to generate modulation schemes that transfer more bits per symbol (e.g. QAM modulation [3], [4]) or provide spectral benefits such as single-sideband (SSB) modulation [5], [6]. Other approaches include using analog circuitry and a digital-to-analog converter (DAC) to change the bias voltage of a semiconductor device connected to the antenna [7], [8].

Many biomedical devices rely on BLE due to its low cost and wide availability [9], but BLE radio power consumption limits miniaturization and implantability. It has been shown

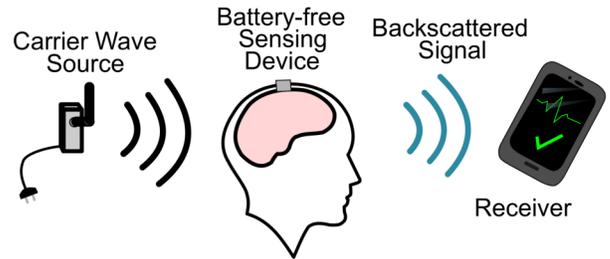


Fig. 1. Example biomedical device leveraging backscatter data uplink.

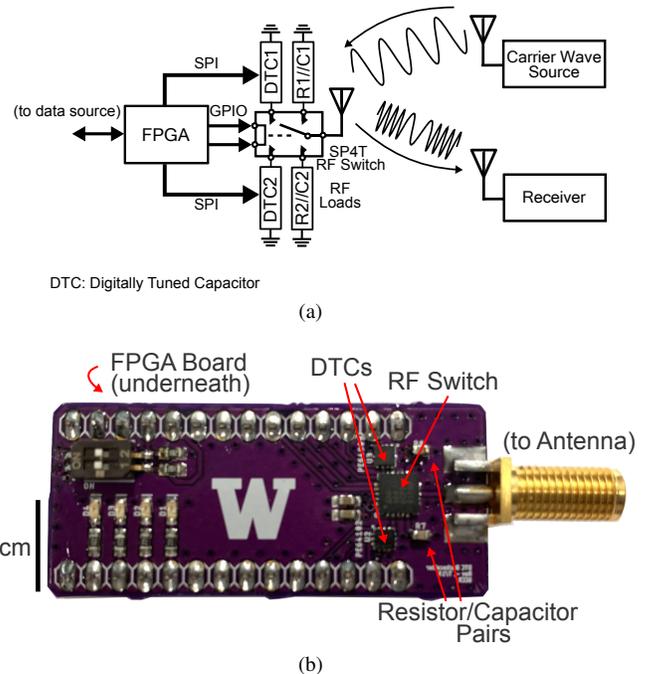


Fig. 2. (a) Block diagram of the SSB BLE backscatter device (b) Device photo

that the radio power consumption of BLE uplinks could be reduced by $>50X$ using a backscatter approach [6], [10]. For a backscatter radio with a typical 50Ω antenna, the ideal M -ary impedance constellation requires inductive reactances. However, inductors are undesirable from a die area and quality factor perspective when a single-chip application

Table 1. Measured SSB BLE Device Power Consumption

	Current (mA)	Power (mW)	% of Total
TinyFPGA BX	9.95	34.83	98.20%
RF Switch	0.06	0.20	0.56%
DTCs	0.12	0.43	1.21%
Total	10.13	35.46	

specific integrated circuit (ASIC) implementation is desired. The all-digital SSB BLE implementation presented here avoids the use of inductors, and has the benefit of an easily trimmable impedance constellation using digitally tunable capacitors only.

II. SYSTEM OVERVIEW & DESIGN

The prototype backscatter device is comprised of a TinyFPGA BX board, using the Lattice Semiconductor iCE40 FPGA, an antenna (L-Com 2 dBi monopole), and a custom printed circuit board (PCB) integrating a CMOS SP4T RF switch (Analog Devices ADG904) and four switched impedances (Fig. 2b). The impedances are implemented using two CMOS digitally tuned capacitors (DTC) (Peregrine Semiconductor PE64909 and PE64102), and two fixed resistor-capacitor pairs. As shown in Table 1, the power consumption of the device is <36 mW from a 3.5 V supply, measured with a precision Keithley power supply. Of the total, 34.8 mW (98.2%) is due to digital logic in the FPGA (Fig.3), and only 600 μ W (1.8%) is consumed by the backscatter modulator. All components are compatible with operation in both the 915 MHz and 2.4 GHz ISM bands. Since the focus of this work is BLE compatibility, only results from the 2.4 GHz band are presented here.

Table 2. Backscatter modulator impedances used for the 2.4 GHz ISM band

Z	Impedance States			DTC Tuning Word
	R Value	C Value	Γ	
Z_0	-	0.962 pF	-0.61 - j0.032	0x04
Z_1	-	3.032 pF	0.36 + j0.01	0x06
Z_2	19.1 Ω	0.5 pF	-0.31 + j0.38	-
Z_3	131 Ω	0.5 pF	0.20 + j0.33	-

A. Impedance Constellation Design

Because on-chip inductors are area-hungry and have poor quality factor (Q), we have designed an impedance constellation using only resistors and capacitors. The initial impedance values for the modulator were chosen based on the methods outlined in [3]. Resistive elements were chosen for two of the impedance states and DTCs were used for the other two elements to provide the flexibility to tune the constellation. The initial impedance values were measured at the reference plane of the SMA connector (Fig. 2b) using a vector network analyzer (VNA). Capacitors (0.5 pF) were added in parallel to the resistive elements. Fig. 4 shows the achievable impedance states as the DTC tuning words are varied across all possible tuning states, while the selected tuning words are listed in Table 2. The particular DTC values were chosen to maximize the distance between symbols while still maintaining the

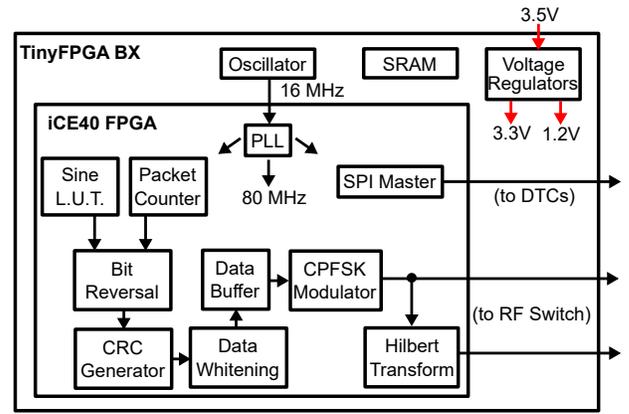


Fig. 3. Block diagram of the digital design on the FPGA

impedance states within one half-plane of the Smith chart. This resulting impedance constellation thus better resembles an inductor-free (R/C only) ASIC implementation.

B. Digital Design

The backscatter device uses an FPGA to process data, generate data packets per the BLE v5.0 specification, and control the RF switch (Fig.3). The FPGA can interface to various sensors, such as biopotential amplifiers for neural recording [1]. In this initial evaluation, a sine-wave look up table (LUT) was used as a proxy for sensor data. The total design uses 4135 logic elements, of which approximately 2000 are dedicated to the sine-wave LUT. The sensor data and a packet counter are formatted into a BLE advertising packet structure and a 24-bit cyclic redundancy check (CRC) is appended before the packet passes through a digital data whitening filter. The data bits are then passed to a modulator block that implements continuous-phase frequency shift keying (CPFSK) modulation with a symbol rate of 1 Mbps and sub-carrier frequencies of 4 MHz and 5 MHz. For SSB operation, a PLL in the FPGA is used to increase the frequency of the 16 MHz external oscillator to 80 MHz. The fast clock enables the FPGA to perform SSB modulation by generating 90 degree-shifted versions of the sub-carrier signals via a Hilbert Transform [6]. The backscattered CPFSK sub-carriers then form a BLE transmission in the desired BLE channel, when an externally supplied CW carrier 4.5 MHz above the desired channel is provided.

III. SIMULATION & MEASUREMENT RESULTS

A. Backscatter Simulations

Matlab simulations were used to analyze the spectrum of DSB and SSB BLE backscattered packets using the measured impedances shown in Fig.4b. A plot of the simulated spectrum is shown in Fig. 5. As expected from SSB modulation, we see a gain of +3 dB in the desired lower sideband (LSB) and attenuation of 8 dB in the undesired upper sideband (USB). Defining the sideband suppression ratio (SSR) as,

$$SSR_{dB} = Gain_{LSB, dB} + Atten_{USB, dB}, \quad (1)$$

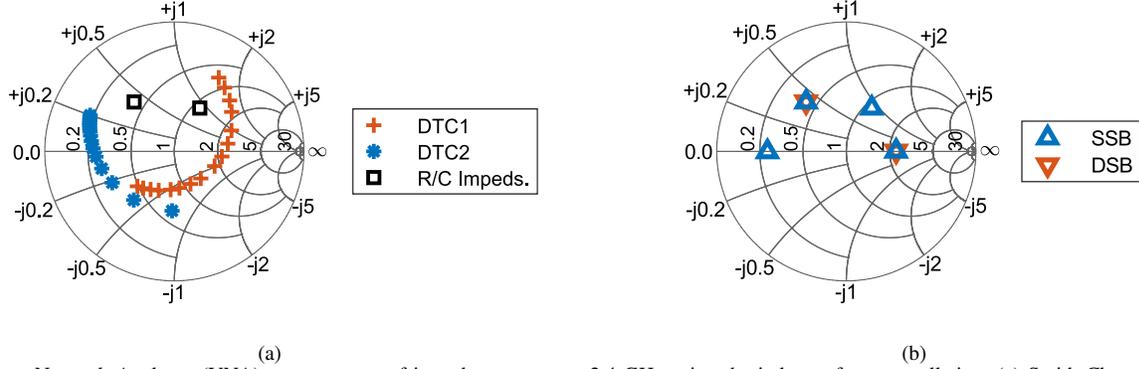


Fig. 4. Vector Network Analyzer (VNA) measurement of impedance states at 2.4 GHz using the inductor-free constellation: (a) Smith Chart of all achievable impedance states, (b) Smith Chart showing the selected impedances for double sideband (DSB) and single sideband (SSB) modulation states. Some modulator impedances in the capacitive half-plane appear in the upper half-plane in this Smith chart, because the measurement plane is defined at the device’s SMA connector.

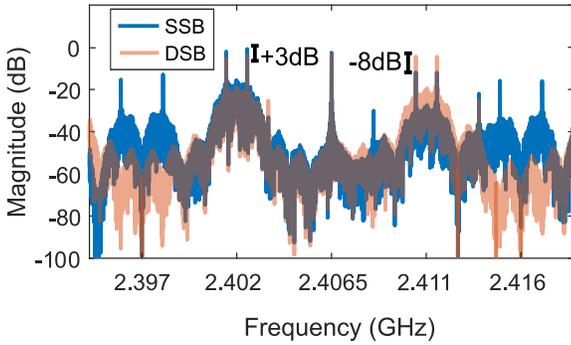


Fig. 5. Plot of the simulated spectrum for DSB and SSB modulation schemes using the measured impedance constellation

we find that the inductor-free digitally tuned capacitance constellation yields an SSR of 11 dB. We note that there is little suppression of the carrier due to the impedance constellation residing in one half-plane of the Smith chart.

B. Cabled Validation

The spectrum of DSB and SSB BLE backscattered packets were measured using the setup shown in Fig. 6a. The measured spectrum is shown in Fig. 6b. We find that the backscatter device achieves a measured gain of 1.9 dB in the desired sideband and a measured attenuation of 8.8 dB in the undesired sideband, yielding a measured SSR of 10.7 dB. The simulation did not include impedance mismatches in the coupler and cabling, to which we attribute the discrepancy between the measured SSR and the Matlab-calculated SSR.

C. Over-the-air Validation

After the SSB BLE implementation was validated in the cabled setup, an over-the-air validation was performed using the measurement setup of Fig. 7a. The backscatter device was programmed to uplink sample values from an sine wave LUT to simulate sensor data. An external CW carrier was

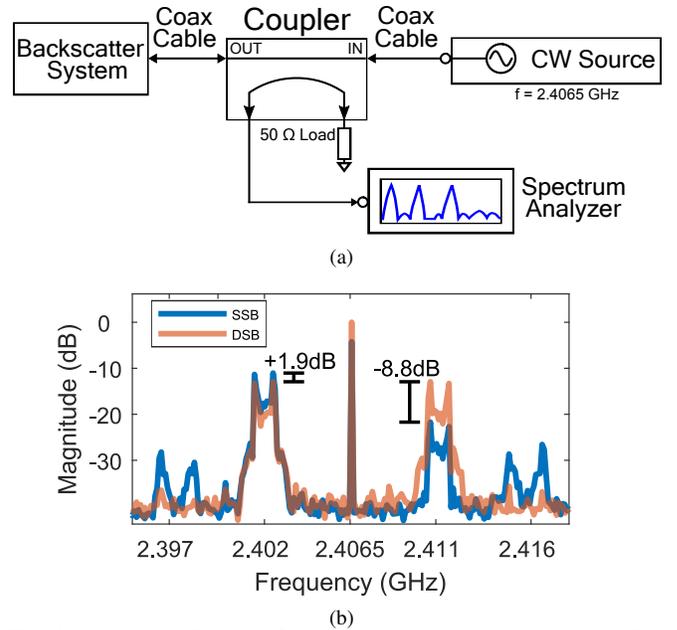


Fig. 6. (a) Block diagram of cabled measurement setup (b) Plot of the measured spectrum for DSB and SSB modulation.

generated at 2.4065 GHz using an RF signal generator and amplifier yielding a carrier power of +20 dBm. Packets were received using an unmodified, off-the-shelf BLE receiver (Nordic Semiconductor nRF51822 development kit), and their contents were analyzed using an open-source packet analyzer (Wireshark) and Matlab. A plot of the sample values contained in the received packets are shown in Fig. 7b. Measurements were conducted on a university campus with significant BLE traffic that likely contributed to the dropped packet observed in Fig. 7b. Packets were also successfully received and processed using a completely unmodified Apple iPad, Apple iPhone, and a Samsung Android smartphone.

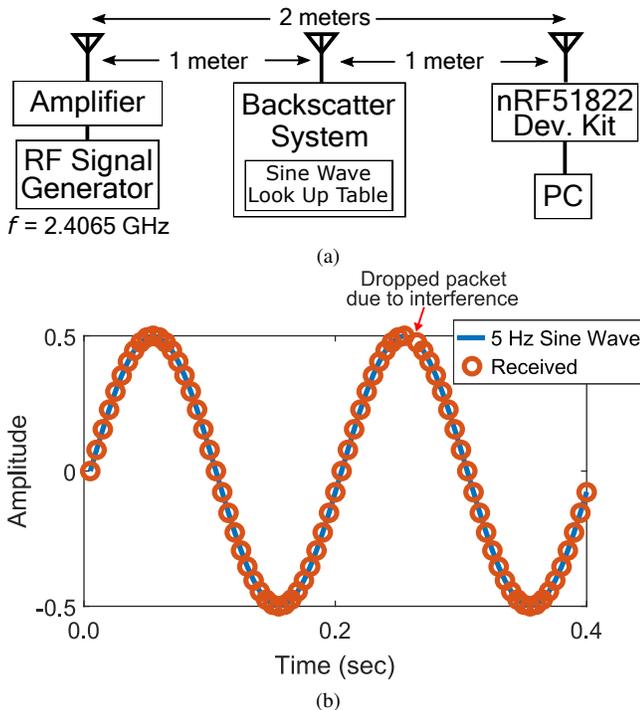


Fig. 7. Over-the-air validation experiment: (a) Measurement setup, (b) Plot sine-wave test data received by the nRF51822 BLE receiver

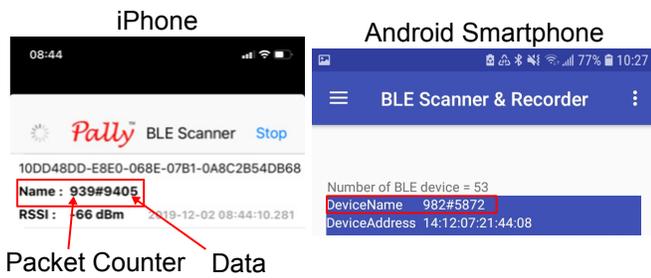


Fig. 8. Screenshots of received packets on unmodified (no modifications to hardware or software) iPhone and Samsung Android smartphones.

IV. CONCLUSIONS & FUTURE WORK

This paper presents a novel all-digital approach for generating single-sideband (SSB) backscatter communication uplinks, using an inductor-free, digitally-tuned capacitance modulator. An example Bluetooth Low Energy (BLE) compatible single-sideband backscatter uplink is described. The FPGA-based approach presented here consumes 35.5 mW, of which 34.8 mW (98.2%) is due to digital logic in the FPGA, and only 600 μ W (1.8%) is consumed by the backscatter modulator. The measured sideband suppression ratio is 10.7 dB. Over-the-air tests demonstrate compatibility with a completely unmodified (neither hardware nor software modifications) iPad, iPhone, Samsung Android Smartphone, and an off-the-shelf BLE chipset from Nordic Semiconductor. This all-digital approach points the way toward future single-chip, inductor-free SSB BLE-compatible backscatter sensors and devices.

Future work includes the integration of the proposed DTC based backscatter modulator approach in a single-chip ASIC implementation targeting applications such as biomedical sensing systems. Additional future work includes the demonstration of M -ary phase shift keying modulation alongside the proposed BLE waveform, so that a single backscatter device can support a high data rate proprietary uplink alongside a lower data rate, standards-based BLE uplink.

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