Hardware-Efficient All-Digital Architectures for OFDM Backscatter Modulators

James D. Rosenthal, and Matthew S. Reynolds,

***Abstract*—Orthogonal frequency division multiplexing (OFDM) backscatter communication promises to enable ultra-low power wireless devices that are robust to time-varying multipath channels. Traditional OFDM transmitters require the use of power-hungry digital-to-analog converters (DACs) and vector modulators to realize the OFDM signal, adding to the complexity and power consumption of wireless sensor nodes. In this work, we compare three all-digital architectures for OFDM backscatter communication that use RF switches and discrete loads to implement digitally controlled single-sideband OFDM backscatter modulators. We present design analysis including simulations and measurements for a selected implementation using five subcarriers having binary phase shift keying (BPSK) modulation at a symbol rate of 250 kSymbols/s, and a throughput of 1.25 Mbit/s with a modulator energy consumption of 160 pJ/bit. We also present a five-subcarrier over-the-air validation with 195 kbps throughput. We demonstrate how the number of RF switch states and the choice of impedances impact the metrics of subcarrier interference ratio and sideband suppression ratio, and we explore how reduced-numeric-precision Inverse Fast Fourier Transform (IFFT) structures impact the theoretical bit-error rate. The all-digital architecture and analysis presented in this paper enables new avenues of low-cost, digital OFDM and multiple-access backscatter communication systems for use in challenging multipath environments.**

***Index Terms*—Backscatter communication, full-duplex radios, internet of things (IoT), orthogonal frequency division multiplexing (OFDM) backscatter, radio frequency identification (RFID)**

I. Introduction

THE potential for energy efficiency offered by backscatter communication has resulted in numerous practical applications, primarily with different single-carrier modulation schemes. By carefully selecting the specific modulator impedances and the sequence in which they are presented to the antenna, researchers have demonstrated analog modulation [2] and digital modulation schemes such as amplitude-shift keying [3], [4], phase-shift keying [5]–[7], frequency shift keying [8]–[10], quadrature phase-shift keying [11], and 16-quadrature-amplitude modulation modulation [12] with data rates as high as 96 Mbits/s and up.

One drawback of single-carrier modulation is decreased reliability in channels with time varying multipath. Conventional active radio standards, such as IEEE 802.11 WLAN, have used multi-carrier orthogonal frequency division multiplexing (OFDM) to overcome these channel impairments. Traditionally, OFDM is implemented using the real and imaginary outputs of an inverse Fast Fourier Transform (IFFT) to control two voltage digital-to-analog converters (DACs) which in turn drive a vector modulator, as shown in Fig. 1(top). This

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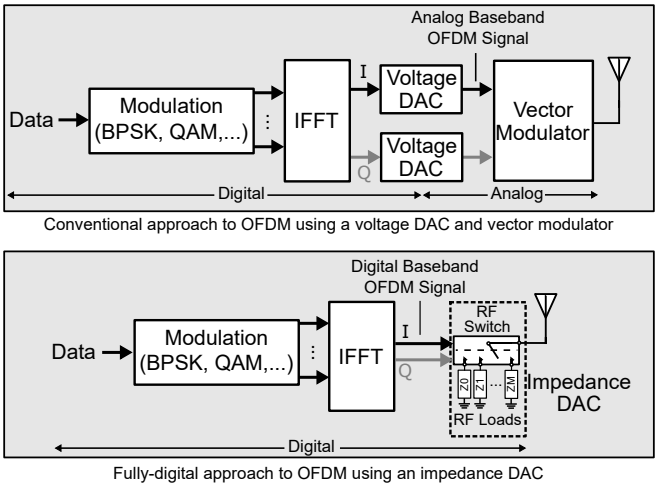

Fig. 1. Comparison of (top) a traditional OFDM architecture using I/Q voltage DACs and a vector modulator and (bottom) the proposed all-digital backscatter OFDM architecture using an RF switch and discrete loads to form a discrete-valued impedance DAC.

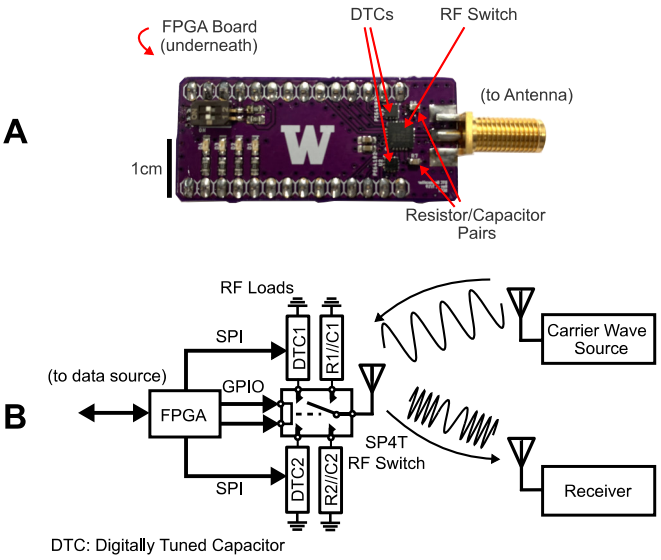

Fig. 2. OFDM backscatter was implemented on an off-the-shelf FPGA and a custom switched-impedance backscatter modulator using digitally-tuned capacitors (DTC) described in [1]. (a) Photo of the backscatter modulator, (b) Block diagram of the backscatter modulator.

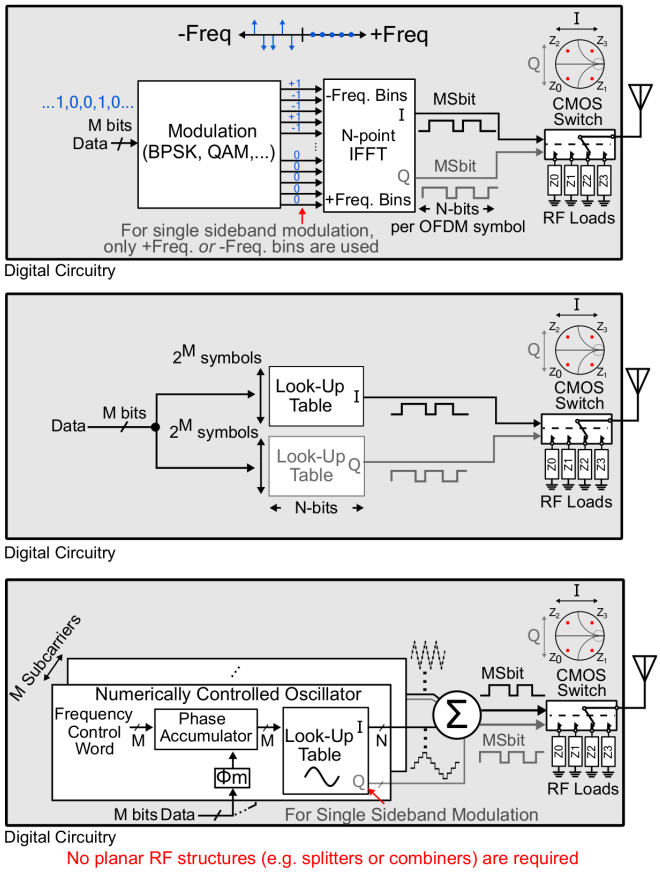

Fig. 3. Three candidate architectures for implementing OFDM backscatter communication with a switched impedance modulator. OFDM subcarriers can be generated using (top) on-the-fly Inverse Fast Fourier Transform (IFFT), (middle) IFFT lookup tables (LUTs), and (bottom) numerically controlled oscillators based on a sine look-up table (LUT).

implementation is relatively power hungry due to the need to run the DACs at a sampling rate sufficient to Nyquist sample the entire OFDM signal bandwidth.

Several recent works have developed building blocks for OFDM backscatter communication, but each still requires the use of digital-to-analog converters (DACs) and high speed lookup tables to compensate for the non-linear impedance-vs.-voltage curves of typical modulators. For example, in [13] pulse-shaping for backscatter communication was explored by using a DAC to control a voltage-variable impedance, such as a field-effect transistor (FET), connected to the backscatter device's antenna. The impedance of such a single-FET modulator is a non-linear function of the applied control voltage and is also strongly influenced by the incident carrier wave (CW) power. In [14], an amplitude-frequency-shift keying (AFSK) OFDM backscatter integrated circuit (IC) was developed. The IC uses direct digital frequency synthesizers to generate distinct subcarrier signals driving R2R DACs that in turn provide gate bias for an array of modulating FETs. OFDM-like backscatter signals were demonstrated in [15], but this work also relied on DACs, FET-based modulators, and tuned RF structures. In these prior works, achieving incident-power-independent impedance states is challenging due to the modulator FET's non-linear dependence on incident power and gate bias voltage. Further, high speed DACs generally have high power consumption, on the order of tens of milliwatts or greater, making them an unfavorable choice for highly energy-constrained wireless devices.

In this work, we present three all-digital architectures for OFDM backscatter communication that can be realized using digital CMOS RF switches as the backscatter modulator elements (Fig. 1 (bottom)). We provide design analysis on a selected architecture, with FPGA-based digital logic driving a custom backscatter modulator printed circuit board (PCB) (Fig. 2) described in [1]. The modulator leverages digitally tuned capacitors (DTCs) to achieve a reconfigurable inductor-free modulator that facilitates prototyping for future application specific integrated circuits (ASICs). This work provides a significant contribution to the field of low power wireless sensing and backscatter communication in the following ways:

- Design and Performance Repeatability: The all-digital architecture produces repeatable impedances across a far broader range of incident carrier wave power than DAC-driven FET modulator architectures.
- Platform Flexibility: The three proposed OFDM backscatter architectures can be implemented in any conventional digital logic device, including field-programmable gate arrays (FPGAs), complex programmable logic devices (CPLDs), microcontroller units (MCUs), and CMOS ASICs. The design analysis of this work provides an understanding of how the design architecture affects digital resource utilization and wireless link performance.
- Protocol Configurability: The proposed OFDM backscatter architectures allow for easy configurability of the physical and link layer communication parameters, such as the number, frequency, and modulation of the subcarriers as well as the desired sideband relative to the incident carrier wave. Well-known OFDM packet structures to mitigate inter-symbol and inter-carrier interference can be easily added.

The outline of this paper is as follows: Section II presents an overview of the proposed OFDM backscatter architectures. Section III presents simulation results for a selected architecture based on an IFFT lookup table (LUT). Section IV presents a comparison between simulated and measured results and an over-the-air validation of this architecture. Finally, Section V presents conclusions and ideas for future work.

II. Architectures for OFDM Backscatter Communication

A. Impedance DAC

In this work, we chose to use a digitally-controlled CMOS RF switch to control the impedance presented to the antenna. Using a switched modulator has several benefits over voltage-controlled variable impedances. The first is that the switch FETs are biased as digitally controlled RF switches that connect externally provided impedances to the antenna, so fluctuations in the incident RF carrier power do not disrupt the modulator impedance. This is a key limitation of previously-described modulators using the FET itself as a variable impedance. Switch based implementations provide

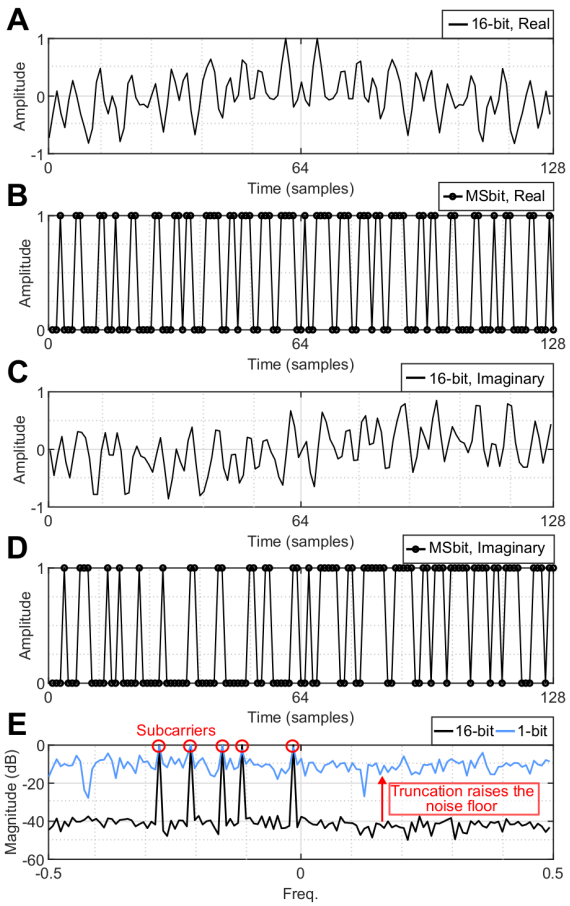

Fig. 4. Simulation of the baseband signals showing the output of a 128-bit IFFT with (a, c) 16-bit resolution and (b, d) the same signal truncated to the most significant bit (MSb): (a), (b) real parts; (c),(d) imaginary parts; (e) Fourier transform of the complex IFFT output comparing a 16-bit resolution signal to the 1-bit truncated signal.

backscatter modulators that can achieve consistent, reliable operation over a wider range of incident carrier wave power. Secondly, the switch is controlled using all-digital logic that is widely available across low-cost MCUs, CPLDs, FPGAs, and ASICs. Once the impedances connected to the switch are determined, there is no need for calibration to achieve repeatable operation. Lastly, CMOS RF switches can achieve data rates of on the order of tens of megabits per second due to their fast switching times [12], [16]. A disadvantage to using CMOS RF switches is that the two-way insertion loss can often be >3 dB, however this can often be improved given careful attention to the switching FET device and process.

An RF switch used to switch between different discrete impedance states can be viewed as an impedance DAC. For example, a single pole-single throw (SPST) switch can be seen as providing 1-bit of impedance resolution. At a constant switching rate, a SPST switch can achieve ON-OFF keying (OOK) or binary phase-shift keying (BPSK) modulations. However, if the switching rate of the SPST is modulated such that one of M different switching rates is selected for each symbol period, then M-ary frequency shift keying (FSK) modulation can be implemented, such as in [10].

A key insight in this work is that multiple simultaneous carrier frequencies can be generated by using multi-tone

TABLE I
RESOURCE ALLOCATION FOR EXAMPLE OFDM BACKSCATTER ARCHITECTURES EMPLOYING FIVE SUBCARRIERS

Architecture	Logic Elements	Multipliers	Block RAM (Bytes)
128-Point Buffered Burst IFFT	3,556	24	1,985
128-Point IFFT LUT	505	0	0
NCO (Full Sine LUT, 2048-point)	1600/subc.	0	0
NCO ($\frac{1}{4}$-wave Sine LUTs, 2048-point)	500/subc.	0	0
NCO (Full Sine LUT, 128-point)	120/subc.	0	0
NCO ($\frac{1}{4}$-wave Sine LUTs, 128-point)	50/subc.	0	0
NCO (Small RAM)	81/subc.	0	60

Values are reported from the Intel Quartus Prime *Analysis & Synthesis* report summary.

symbol sequences to actuate the RF switch. These symbol sequences correspond to the digital baseband OFDM signal of Fig. 1(bottom). Using such symbol sequences can enable even a one-bit impedance DAC, e.g. an SPST switch, to generate orthogonal subcarriers.

B. OFDM Backscatter Architectures

A challenge when implementing OFDM is balancing the desire for a fast, high-resolution IFFT with the limited hardware resources and power available in embedded systems. An IFFT block has many different design parameters, including the number of bins, the bit width and fractional length for data and twiddle factors, and the radix of the butterfly modules. With each of these parameters comes trade-offs in computational speed and resource utilization. There has been significant research in hardware efficient algorithms designed for use in OFDM [17]. For example, in applications that have unused bins in the IFFT, "pruning" can be used to reduce the complexity of the IFFT block [18]. Additionally, for low resolution applications, smaller bit widths and fractional parameters can be used to reduce the number of logic elements and memory needed for a particular design. To better understand the resources required for implementing OFDM backscatter, we present three architectures for generating the requisite digital baseband OFDM signals: an on-the-fly inverse Fast Fourier Transform (IFFT) architecture, a IFFT Look-Up Table (LUT) architecture, and a numerically controlled oscillator (NCO) architecture, as shown in Fig. 3.

1) IFFT-based Architecture: OFDM backscatter communication can be generated using the on-the-fly IFFT-based architecture shown in Fig. 3 (top). This architecture closely resembles a traditional OFDM implementation, except it replaces the voltage DACs and vector modulator by an RF switch and two or more discrete RF loads. In this configuration, data bits are passed through a modulation block that maps bits to M complex-valued symbols. The symbols are then arranged in parallel and input into the desired subcarrier frequency bins of an N-point IFFT, while the undesired subcarrier frequency bins are set to zero. If the input to the IFFT is symmetric, with the same inputs being applied to the corresponding positive and negative frequency bins, then the frequency spectrum will be double sideband (DSB) and the IFFT output will be a real-valued time domain signal that is N samples long. If the input to the IFFT is asymmetric with inputs only applied to the positive or negative frequency bins, then a single sideband (SSB) frequency spectrum will be generated. The IFFT output

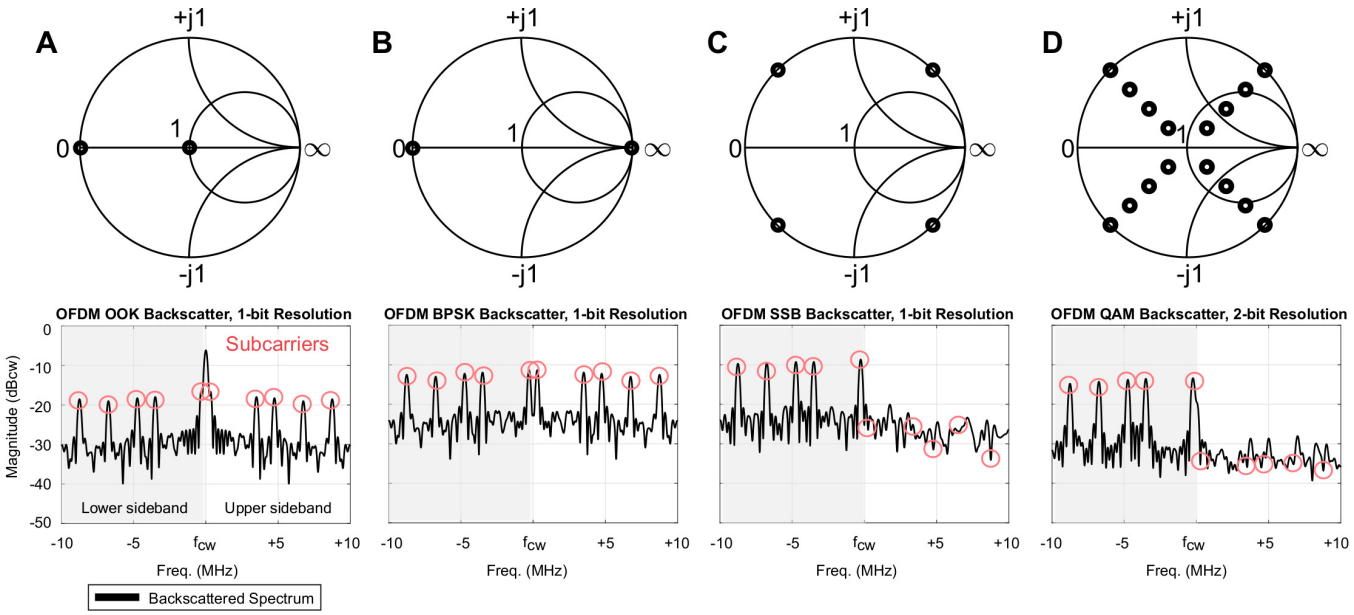

Fig. 5. Simulation of OFDM backscatter spectral power using five subcarriers and different impedance configurations: (a) two real-valued impedances that are absorptive and reflective, (b) two real-valued reflective impedances that are 180 degrees out of phase, (c) four complex-valued reflective impedances that are 90 degrees out of phase, enabling single sideband modulation, and (d) sixteen complex-valued reflective impedances. (a)-(b) can be implemented with a two-throw switch, (c) with a four-throw switch, and (d) with a sixteen-throw switch. Spectral plots are in units of power relative to the incident carrier wave (abbreviated as dBcw).

in this case will be complex, composed of a real (I) and imaginary (Q) component that are each N samples long. Each sample will have its amplitude coded in one or more bits.

For an RF switch with S switch states, $c = \log_2(S)$ control signals are required. The amplitude of the IFFT output can be truncated such that c total bits are obtained. For example, a single pole-four throw (SP4T) switch requires two control bits. In this case, the most-significant bit (MSB) from each of the I and Q signals can be used to actuate the switch among its four possible states. The digital baseband signals for this example are shown in Fig. 4. As a result of the I and Q signals being truncated in resolution, the wideband noise floor is elevated relative to an implementation having more switch states.

2) Simplified IFFT LUT Architecture: Implementing an on-the-fly IFFT block in a device allows for significant flexibility, but it comes at the cost of hardware complexity and additional power consumption. IFFT implementations in digital logic generally require multipliers and block memory for storing intermediate calculations as well as LUTs for the complex exponential roots of unity, also known as twiddle factors. For example, a 128-point Radix-2 Buffered-Burst IFFT generated using the Intel Quartus Prime FPGA design software uses 24 multipliers, nearly 2,000 Bytes of RAM and over 3,000 logic elements (TABLE I). Certain low cost, low power digital devices like the Lattice Semiconductor iCE40 FPGA [19] and MachXO2 [20] are appealing platforms for backscatter communication due to their low static power consumption, but they lack dedicated multiplier blocks and requisite number of logic elements to compute the IFFT. These hardware constraints can be overcome though by pre-calculating OFDM backscatter symbols and storing them in LUTs, reducing resources at the cost of real-time configurability. A block diagram of this implementation is shown in Fig. 3 (middle). In this implementation, the incoming data bits are used to select the corresponding OFDM symbol from the pre-generated LUT. As TABLE I shows, this implementation requires only 17% of the logic elements of an IFFT and no multiplier or block RAM.

3) NCO Architecture: An alternative to IFFT-based architectures is to use a dedicated NCO for each subcarrier, as shown in Fig. 3 (bottom). In this approach, the outputs of each NCO are added together in a digital adder, after accounting for potential bit growth. The c MSbits are then used to actuate the RF switch. For applications that require real-time configurability for a small number of subcarriers, this is an appealing choice. Each NCO is characterized by its phase resolution, i.e. number of samples per sinusoidal period N_{NCO}, and the amplitude resolution, i.e. number of bits per sample. The output frequency is then controlled by a frequency control word, f_{ctl}, such that the output frequency is $f_{\text{out}} = \frac{f_{\text{ctl}}}{N_{\text{NCO}}} * f_{\text{s}}$, where f_{s} is the sample rate.

In the simplest implementation where an NCO is built using a full sinusoidal LUT with, for example, 11-bit phase resolution and 16-bit amplitude resolution, each subcarrier requires approximately 1600 logic elements. By exploiting the symmetry in a sinusoidal signal, however, it is possible to generate the same signal using a $\frac{1}{4}$-wave LUT with significant complexity savings. Other implementations exist for NCOs that trade off between logic elements, multipliers, and block RAM [21]. TABLE I outlines the observed resource utilization for three different NCO architectures.

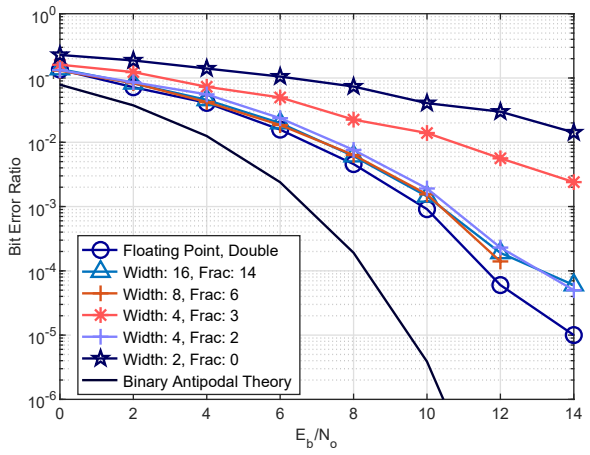

Fig. 6. Plot of simulated of OFDM backscatter BER versus $\frac{E_b}{N_0}$ for different IFFT fixed-point bit resolutions in terms of width and fractional length.

III. Simulating OFDM Backscatter Communication

A. Effects of Impedance Constellation on OFDM Backscatter Spectrum

In all of the OFDM Backscatter architectures, the choice of the RF switch and the impedances connected to it will impact the backscattered frequency spectrum. Numerical simulations were performed to explore the effects that number of RF switching throws and impedance values would have. Simulations were performed in MathWorks MATLAB R2018a software. In the simulations, the simplified IFFT LUT architecture was used based on a 128-point IFFT. The simulations used a symbol rate of 250 kHz, a sample rate of 32 MHz, and five subcarriers (250 kHz, 3.5 MHz, 4.75 MHz, 6.75 MHz, and 8.75 MHz). Each subcarrier was modulated using BPSK modulation, leading to 32 possible OFDM symbols.

Four different RF switch configurations were simulated, as shown in Fig 5. The first two simulation cases used single pole-single throw (SPST) RF switches, with one simulation using absorptive and reflective impedance states and other using two reflective states 180 degrees out of phase. For these two simulations, only the in-phase (I) signal was used to actuate the RF switch, yielding an impedance DAC resolution of one-bit. The third simulation case represented a single pole-four throw (SP4T) RF switch and used four reflective impedance states that were 90 degrees out of phase relative to adjacent states. This situation simulated single sideband backscatter modulation. Both the in-phase (I) and quadrature (Q) control signals were used, each with one-bit resolution, as shown in Fig. 4. The fourth simulation case simulated a single pole-sixteen throw (SP16T) RF switch. The impedance values were chosen to implement single sideband modulation using the in-phase (I) and quadrature (Q) control signals with two-bit resolution each.

The backscatter power spectrum was estimated for each simulation case to compare performance of the different switch and impedance configurations. The power spectra were estimated by calculating the power spectral density (PSD), $S(f) = \mathscr{F}[\bar{R}(\tau)]$ and multiplying it by the estimated noise bandwidth of the window, where $\mathscr{F}[]$ denotes the Fourier Transform and $\bar{R}(\tau)$ denotes the average auto-correlation of the OFDM time-series samples.

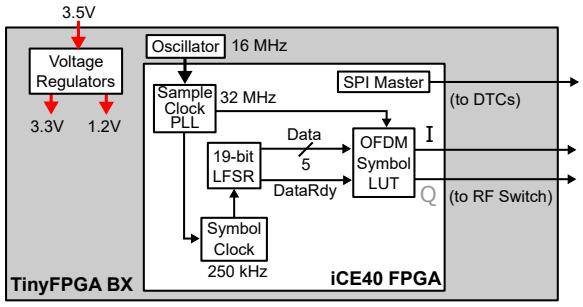

Fig. 7. Block diagram of the FPGA implementation of the IFFT LUT architecture for OFDM backscatter communication. A 16-bit linear feedback shift register (LFSR) was used to produce pseudo-random data for transmission.

From the power spectrum plots of Fig. 5, we can make a few key observations. Firstly, single sideband (SSB) backscatter modulation in (c) had the strongest subcarrier power levels with a maximum of -14.7 dB relative to the incident carrier wave (abbreviated as dBcw). BPSK backscatter modulation in case (b) had the second highest subcarrier power at -17.3 dBcw, while 16-QAM in case (d) was -18 dBcw and OOK in case (a) was -21 dBcw. Given that the reflected power is a function of the vector distance between impedance states, these results are as expected.

Secondly, we can examine the subcarrier interference ratio (SIR) by comparing the worst-case relative power levels of spurious tones between subcarriers to the power levels of the subcarriers. The SIR is found to be -6.7 dB, -8.4 dB, -10.2 dB, and -11.1 dB for cases (a)-(d), respectively. This result demonstrates that SIR appears to improve based on two factors: (1) as the minimum distance between reflection states, $|\delta\Gamma_{\text{min}}|$, increases, and (2) as the resolution of the impedance DAC increases from one bit in cases (a) and (b) to two bits in case (c) and to four bits in case (d).

Thirdly, for cases (c) and (d) we can calculate the sideband rejection ratio (SRR) by comparing to the DSB modulation from case (b). SRR is calculated as the ratio of gain in the desired sideband relative to the attenuation in the undesired sideband at a given subcarrier offset frequency:

$$SRR_{\text{dB}} = \frac{\text{Subcarrier Gain (dB)}}{\text{Subcarrier Attenuation (dB)}} \tag{1}$$

We find that SSB backscatter modulation in case (c) achieves an SRR of 17.7 dB while 16-QAM backscatter modulation in case (d) achieves an SRR of 21.5 dB. The SRR does not tell the entire story though. Despite case (d) achieving a higher SRR, the subcarrier gain in the desired sideband is actually negative, decreasing from a maximum of -17.3 dBcw in case (b) to a maximum of -18 dBcw in case (d). This can likely be attributed to the greater $|\delta\Gamma_{\text{min}}|$ in case (b) [22]. Interestingly, the attenuation of the subcarriers in the upper sideband is 30 dB in the worst case for case (d) while it is 25.4 dB in the worst case for (c), yielding a difference of 4.6 dB.

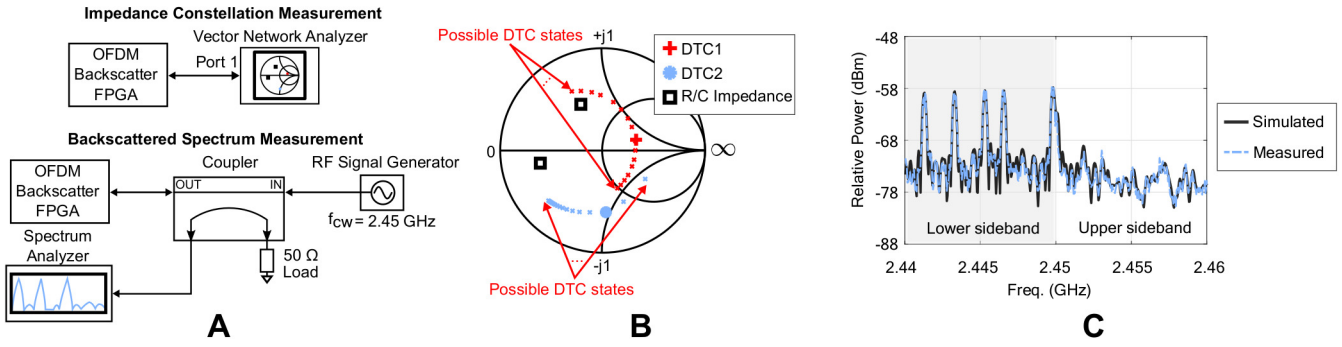

Fig. 8. Measurement setup and results using four complex-valued impedances for SSB OFDM backscatter: (a) Diagram of the cabled setup used to measure the impedance constellation (top) and backscattered spectrum (bottom) of the OFDM backscatter FPGA, (b) Smith chart showing the measured impedances of the backscatter modulator normalized to 50 Ω. The impedances used for the measurement are shown with larger dots or crosses, while the possible DTC states are shown with smaller dots or crosses. (c) Comparison of the simulated backscatter spectrum using the measured impedance values and the measured spectrum from the OFDM backscatter FPGA.

B. Bit-error Ratio Simulations

Bit-error ratio (BER) simulations were performed to investigate how resolution in the IFFT affects data transmission. The simulations used the on-the-fly IFFT architecture of Fig. 3 (top). The IFFT was implemented in Matlab as a 128-point Radix-2 IFFT algorithm using fixed-point data. The fixed-point data was defined by the total bit width and the fractional length. These parameters were applied to the data as well as the twiddle factors, which are pre-calculated values of a unity magnitude complex exponential at different phase angles that are needed to calculate the IFFT. For transmitting data, five subcarriers with BPSK modulation were used, and four ideal reflective states were assumed for the backscatter modulator, as in the simulation of Fig. 5(c). The data was passed through an additive white Gaussian noise channel, and the received symbols were processed using a coherent receiver assuming perfect synchronization. For each value of the energy-per-bit-to-noise-ratio, $\frac{E_b}{N_0}$, either 10^6 bits were transmitted or 200 bit errors accumulated, whichever came first. A plot of simulation results is shown in Fig. 6. In this simulation framework, OFDM backscatter in general performs approximately 4.5 dB worse than the theoretical binary antipodal modulation for independent subcarriers in a non-fading channel. This decrease in performance is likely due to the non-linear bit truncation occurring between the IFFT and the backscatter modulation, which generates residual wideband noise, harmonics and inter-modulation distortion. Among the backscatter signals simulated, the case using data and twiddle factors of type floating-point double performed the best, as expected, given that it provides the highest resolution of the signal.

Surprisingly, comparable BER performance is achieved for bit resolutions as low as four total bits with two fractional bits. BER performance then severely degrades for the cases of four total bits with three fractional bits ("Width: 4, Frac: 3") and two total bits with zero fractional bits ("Width: 2, Frac: 0"). These results suggest an interesting opportunity for OFDM backscatter implementations to leverage significantly reduced IFFT implementations. Not only can the data and twiddle word sizes be reduced, but many of the arithmetic cycles can be eliminated since in a single sideband implementation with relatively few carriers, many of the IFFT calculations result in zeros or near-zero values.

IV. Measurements & Results

Measurements were performed to validate the power spectrum and wireless uplink capabilities of an OFDM backscatter design. The measurements were performed by implementing the simplified IFFT LUT architecture previously mentioned on a TinyFPGA BX [23], an open source hardware platform that uses a Lattice Semiconductor iCE40 FPGA. A block diagram of the digital design is shown in Fig. 7. The digital design was written in the Verilog hardware definition language and was comprised of a 19-bit linear feedback shift register (LFSR) to generate a pseudo-random data stream, a Symbol Clock generator set to trigger each new symbol at a 250 kHz symbol rate, and an OFDM Symbol LUT. The LUT was generated from 128-point IFFT and contains 64 total symbols each consisting of 128 samples. 32 of the symbols corresponding to the in-phase (I) output and 32 correspond to the quadrature (Q) output. Additionally, a serial peripheral interface (SPI) driver is used to initialize the backscatter modulator's DTCs on power-up.

A. Backscatter Modulator Design

A custom PCB was designed to interface the backscatter modulator to the FPGA. The backscatter modulator is implemented using a CMOS SP4T RF switch (Analog Devices ADG904 [16]) controlled by the FPGA, as shown in Fig. 2(b). The RF switch connects one of four impedances to the antenna. The impedances are implemented using two CMOS DTCs (Peregrine Semiconductor PE64101 and PE64909 [24]), and two fixed resistor-capacitor pairs. DTCs were used to

TABLE II
Backscatter Modulator Impedances Used for the 2.4 GHz ISM Band

Z	Impedance States R Value	C Value	Γ (Cartesian & Polar)	DTC Word
Z_0	-	2.5 pF	0.02 - j0.70 (0.70∠272°)	0x02
Z_1	-	1.45 pF	0.41 + j0.10 (0.42∠13°)	0x08
Z_2	131 Ω	0.5 pF	-0.21 + j0.46 (0.51∠115°)	-
Z_3	19.1 Ω	0.5 pF	0.61 + j0.12 (0.62∠191°)	-

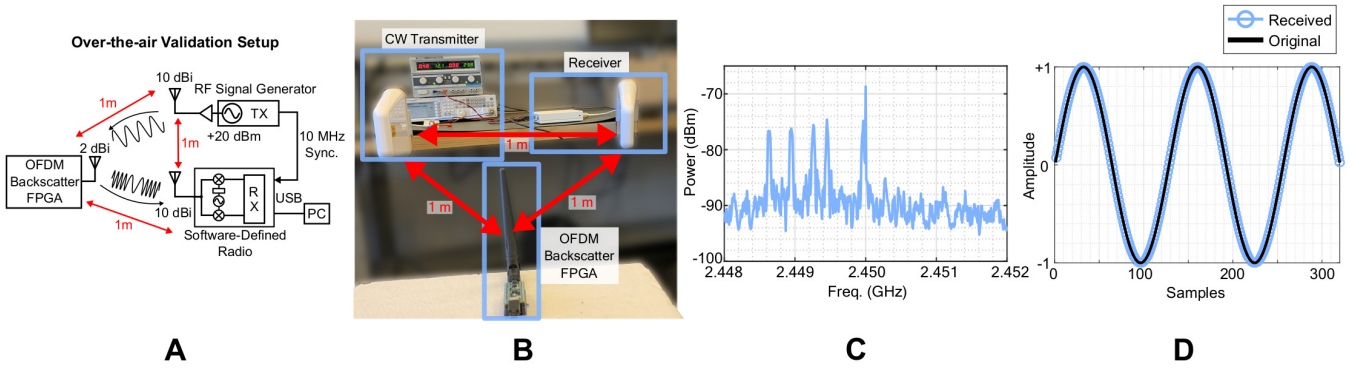

Fig. 9. Measurement setup and results of over-the-air testing: (a) Diagram of the wireless test setup used to uplink data, (b) Photo of the test setup in a lab environment, (c) Measured over-the-air OFDM backscatter spectrum, (d) Measured over-the-air vs. original sampled-sine test data payload showing good agreement. No bit errors were observed in this data set.

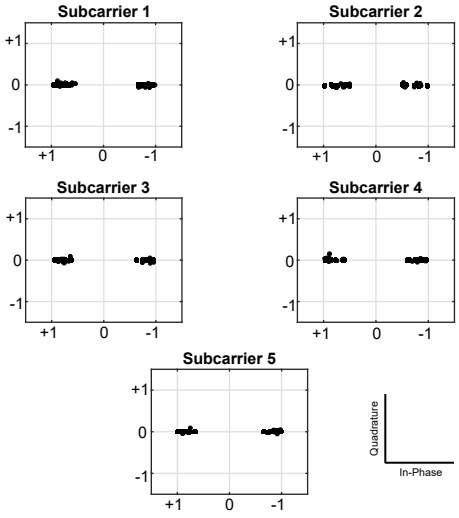

Fig. 10. Subcarrier BPSK constellations from the over-the-air validation.

achieve a reconfigurable inductor-free modulator that facilitates prototyping and design for future application specific integrated circuits (ASICs). The reflection coefficient of each impedance was measured at the reference plane of the antenna connector (Fig. 2(a)) using a calibrated Agilent N5222A vector network analyzer (VNA) (Fig. 5(a)). The tuning word for each DTC was iteratively reprogrammed until the reflection coefficients approximated the ideal SSB backscatter constellation in Fig. 5(c). A summary of the specific impedance values and DTC tuning words is presented in Table II and the measurement setup and Smith chart of the measured modulator impedance values at 2.45 GHz is shown in Fig. 8(a) and (b), respectively.

B. Modulator Power Consumption

The power consumption of the total OFDM Backscatter FPGA was measured with a precision Keithley power supply. The total power consumption (static + dynamic) of both the FPGA board and backscatter modulator PCB was <33.6 mW from a 3.5 V supply. Of the total power 33.0 mW (98.2%) is due to digital logic in the FPGA (Fig. 7), and only 600 μW (1.8%) is consumed by the backscatter modulator. Within the backscatter modulator PCB, the ADG904 RF switch consumed 200 μW while the DTCs together consumed 400 μW of power.

C. Measured Backscattered Spectrum

The OFDM backscatter spectrum was measured using the setup shown in Fig. 8(a). The OFDM backscatter FPGA assembly was connected to the output port of a Mini-Circuits ZABDC20-252H-S+ coupler using a coaxial cable. An Agilent N5181A RF signal generator was connected to the input port of the coupler and configured to generate a pure carrier wave tone at 2.45 GHz and -20 dBm RF power. The output coupled port of the coupler was connected to an Agilent N9320B spectrum analyzer, with attenuation set to 0 dB and a resolution bandwidth of 100 kHz. The input coupled port of the coupler was terminated with a 50 Ω load. With the signal generator turned on, a pseudo-random sequence of OFDM symbols was generated using the 19-bit LFSR on the FPGA. A plot of the measured backscattered spectrum is shown in Fig 8(c). Overlaid on the plot is the simulated spectrum using the measured impedances shown in (b). As the plot shows, the measured spectrum shows good agreement with the simulation.

D. Over-the-air Validation

A wireless over-the-air measurement was performed to validate that OFDM backscatter symbols can be successfully demodulated. For the measurement, a bi-static backscatter communication setup with 1 meter spacing was used, as depicted in the block diagram and photo of Fig. 9(a) and (b), respectively. The external carrier wave (CW) was generated at 2.45 GHz using an Agilent N5181A RF signal generator with 0 dBm output power, a Mini Circuits ZRL-3500+ RF amplifier with a specified gain of 20 dB, and an L-Com HG72710LP-NF log periodic antenna with a specified gain of 10 dBi. The receiver was implemented using an Ettus Research USRP B210 software-defined radio (SDR), and an L-Com HG72710LP-NF log periodic antenna. The internal clock of the SDR was synchronized to the RF signal generator via a 10 MHz synchronization signal. A desktop PC running GNU Radio Companion ran the SDR and performed down conversion, I/Q balancing, sample and symbol synchronization, and decoding with a sample rate of 20 MSps. The OFDM backscatter FPGA was programmed using the design from Fig. 7 with two modifications: (1) the sample clock PLL frequency was reduced to 5 MHz in order to accommodate the

TABLE III
COMPARISON OF STATE-OF-THE-ART OFDM BACKSCATTER DESIGNS

	Kimionis et al., 2016 [13][a]	Tang et al., 2018 [14]	Correia et al., 2018 [15]	**This Work, 2020**
Backscatter Modulator	FET/PIN Diode	FET	FET	**CMOS Switch**
Modulator Control Signal	Analog	Analog	Analog	**Digital**
Voltage DACs Required	Yes	Yes	Yes	**No**
No. of Subcarriers Demonstrated	N/A	4	4	**5**
Subcarrier Modulation	N/A	AFSK	4-QAM	**BPSK**
Demonstrated Operating Frequency	915 MHz	5.8 GHz	2.4 GHz	**2.4 GHz**

[a]Did not explicitly demonstrate OFDM backscatter.

maximum reliable sampling rate of the SDR and PC, and (2) the LFSR was replaced with a sinewave LUT (15-bit amplitude resolution, 128-bit phase resolution) to provide a realistic sensor-data-like payload. The sinewave LUT contained all 32 possible OFDM backscatter symbols and could thus be used to determine whether a receiver could distinguish each unique symbol. The measured over-the-air power spectrum is shown in Fig. 9(c) showing the OFDM backscatter subcarriers. The spectrum was measured using an Agilent N9320B spectrum analyzer with a resolution bandwidth of 1 kHz, the maximum hold function enabled, and averaging enabled over 10 sweeps. Several seconds of wireless data were captured, and a plot of the received samples is shown in Fig. 9(d) overlaid with the original samples. Plots of the individual subcarrier BPSK constellations are shown in Fig. 10. Good agreement can be observed between the received and original samples, and no bit errors were detected, validating the feasibility of using OFDM backscatter to wirelessly uplink data.

V. CONCLUSIONS & FUTURE WORK

This work introduces three all-digital architectures for OFDM backscatter modulation, as well as design analysis, simulations, and measurements for a hardware-efficient IFFT LUT architecture using five subcarriers with BPSK modulation to obtain a throughput of 250 kSymbols/s (1.25 Mbits/s). The hardware implementation uses a low-cost, open-source FPGA platform and a backscatter modulator on a custom PCB. The digital design requires 505 logic elements with no multipliers nor any block RAM. Measurements found that the total power consumption of the device was less than 33.6 mW, dominated by FPGA static power consumption, with a backscatter modulator power consumption of only 200 μW, yielding a modulator energy consumption of 160 pJ/bit. RF measurements using a cabled backscatter setup found good agreement between the physical design and simulated backscattered spectrum. Wireless over-the-air measurements validated that data can be successfully recovered without error from the OFDM backscatter symbols.

Simulations of different backscatter modulator configurations were performed to determine the impact of impedance DAC resolution on the backscattered OFDM spectrum. In general, it was found that the highest backscattered subcarrier power is achieved using single sideband backscatter modulation with > 2 modulator states and the greatest possible distance between impedance states. As the number of modulator states is increased, the impedance DAC resolution increases and the subcarrier interference ratio (SIR) and sideband rejection ratio (SRR) similarly increase. Interestingly, as the number of modulator states increases from four to sixteen, the average distance between impedance states decreases, decreasing the total backscattered power. This suggests that one should carefully consider the increased cost and power consumption required to implement e.g. a 16-state backscatter modulator for OFDM implementations.

Additionally the OFDM backscatter BER performance was simulated using different fixed-point word resolutions in the IFFT. These simulations revealed that comparable performance (within approximately 1 dB for BER of 10^{-4}) can be achieved between bit lengths of 4 to 16 bits. This suggests that optimal IFFT architectures can be developed for backscatter radios that could further reduce resource utilization and power consumption.

The designs and analysis in this paper point the way toward low-complexity, low power wireless sensor nodes leveraging OFDM backscatter. Future work will explore physical and link layer schemes using the architectures presented here. With control of the subcarrier placement and modulation, multi-carrier, multi-protocol backscatter uplinks could be implemented to improve data throughput, multiple access, resilience to interference, and compatibility with custom and off-the-shelf receivers. Additionally, based on our findings that OFDM backscatter can operate with a low-resolution IFFT, optimizations can be investigated to further reduce resource utilization and quantify performance in non-ideal channels. Such a low-resource IFFT could greatly expand the applicability of low power, highly configurable OFDM backscatter based wireless sensors.

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